

FIG. 1

(1)	1ST DATA a	0	1	0	1
	1ST DATA b	0	0	1	1
<hr/>					
	2-BIT DATA	'00'	'01'	'10'	'11'
(2)	1ST OPERATION (a NAND b)	1	1	1	0
	2ND OPERATION (NOT b)	1	1	0	0
	3RD OPERATION (a NOR b)	1	0	0	0
	<hr/>				
	NO. OF 1	3	2	1	0
(3)	DATA	THRESHOLD VALUE			
	'00'	V0 - 3Va			
	'01'	V0 - 2Va			
	'10'	V0 - Va			
	'11'	V0 (=ERASE LEVEL)			

FIG. 2

c	0	0	0	1	(READ LEVEL: HIGH)
d	0	0	1	1	(READ LEVEL: MEDIUM)
f	0	1	1	1	(READ LEVEL: LOW)
<hr/>					
$\bar{d}$ NAND f	1	0	1	1	
$(\bar{d}$ NAND f) NAND $\bar{c}$	0	1	0	1	= a
d	0	0	1	1	= b

FIG. 3

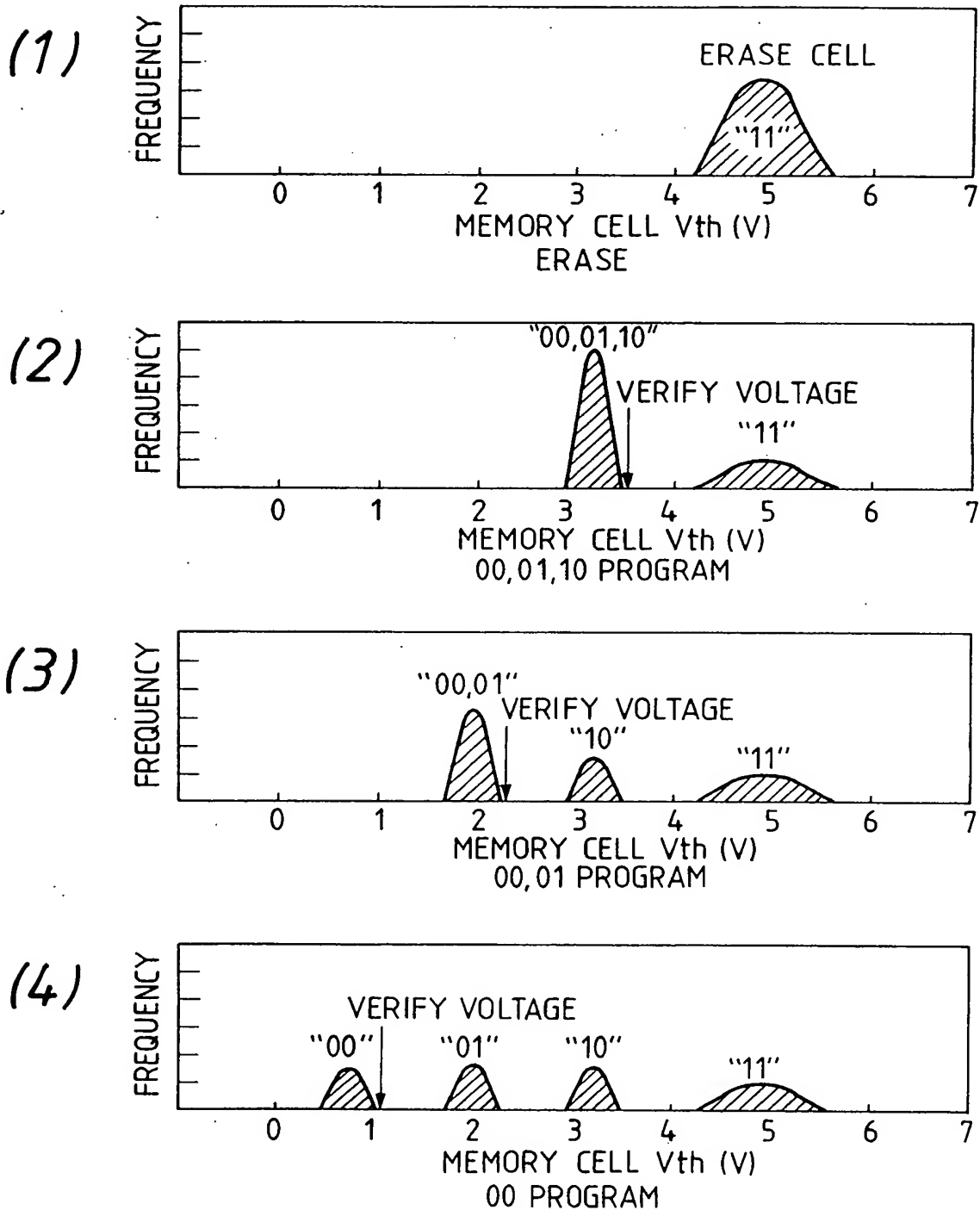


FIG. 4

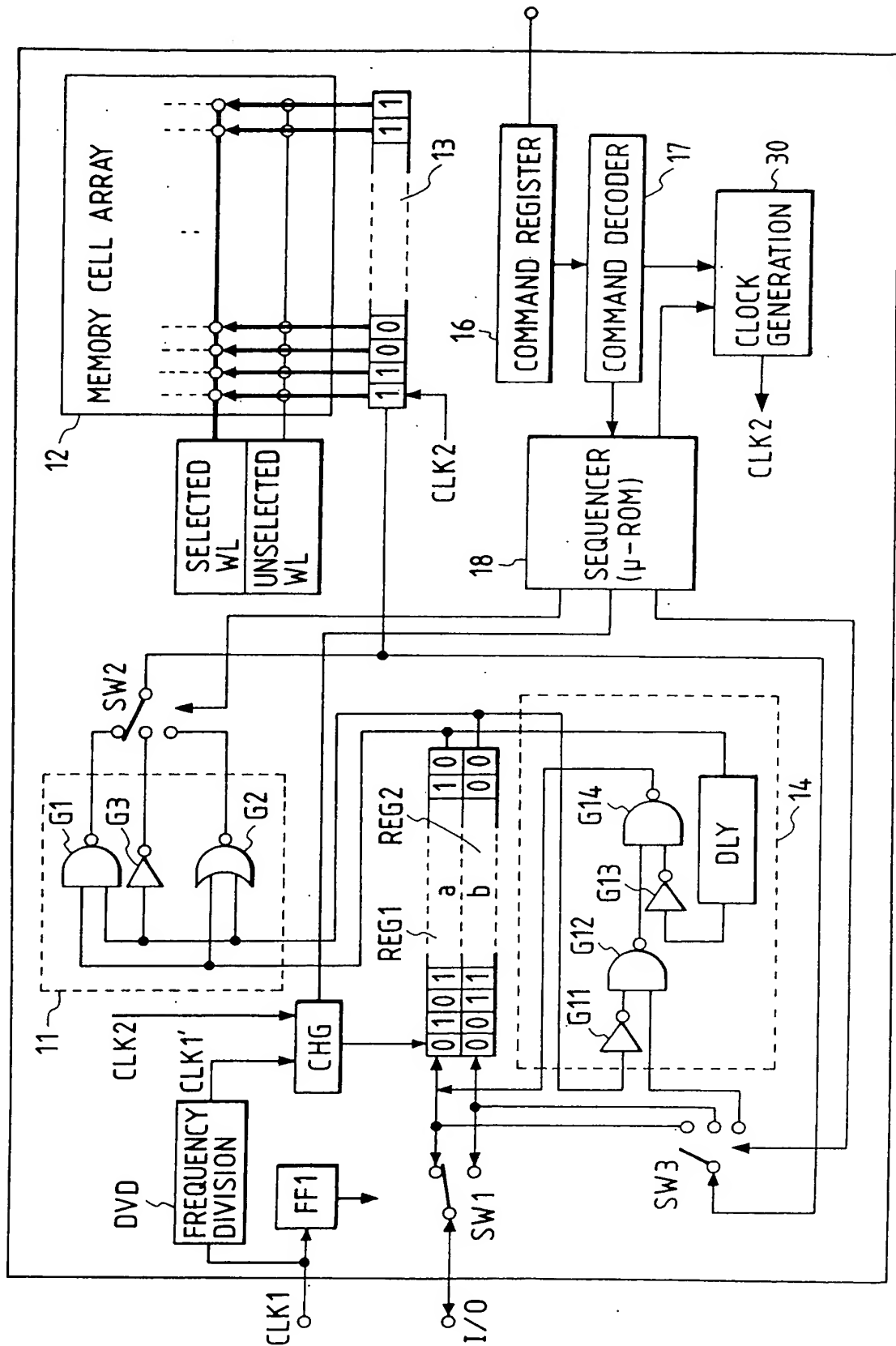


FIG. 5

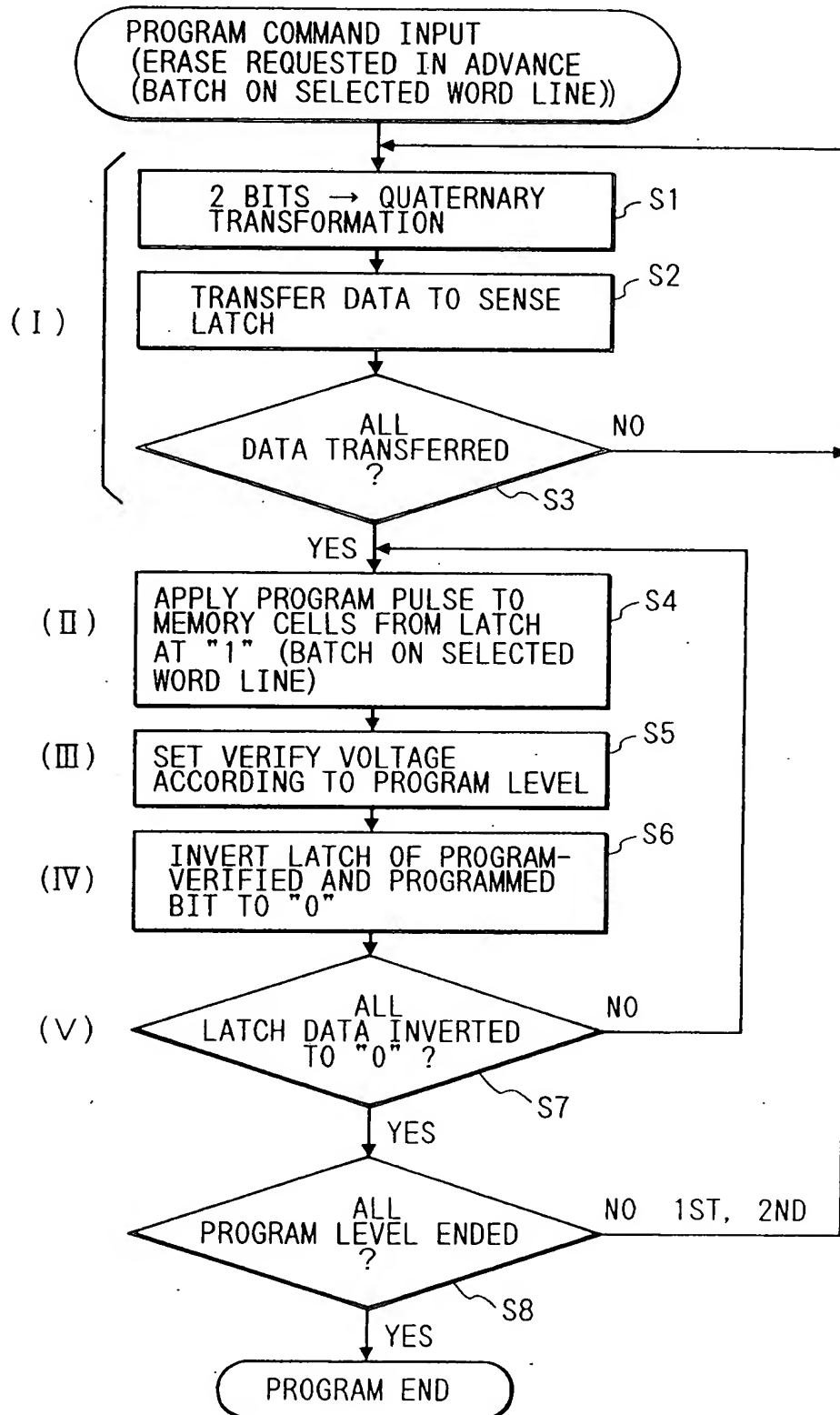


FIG. 6

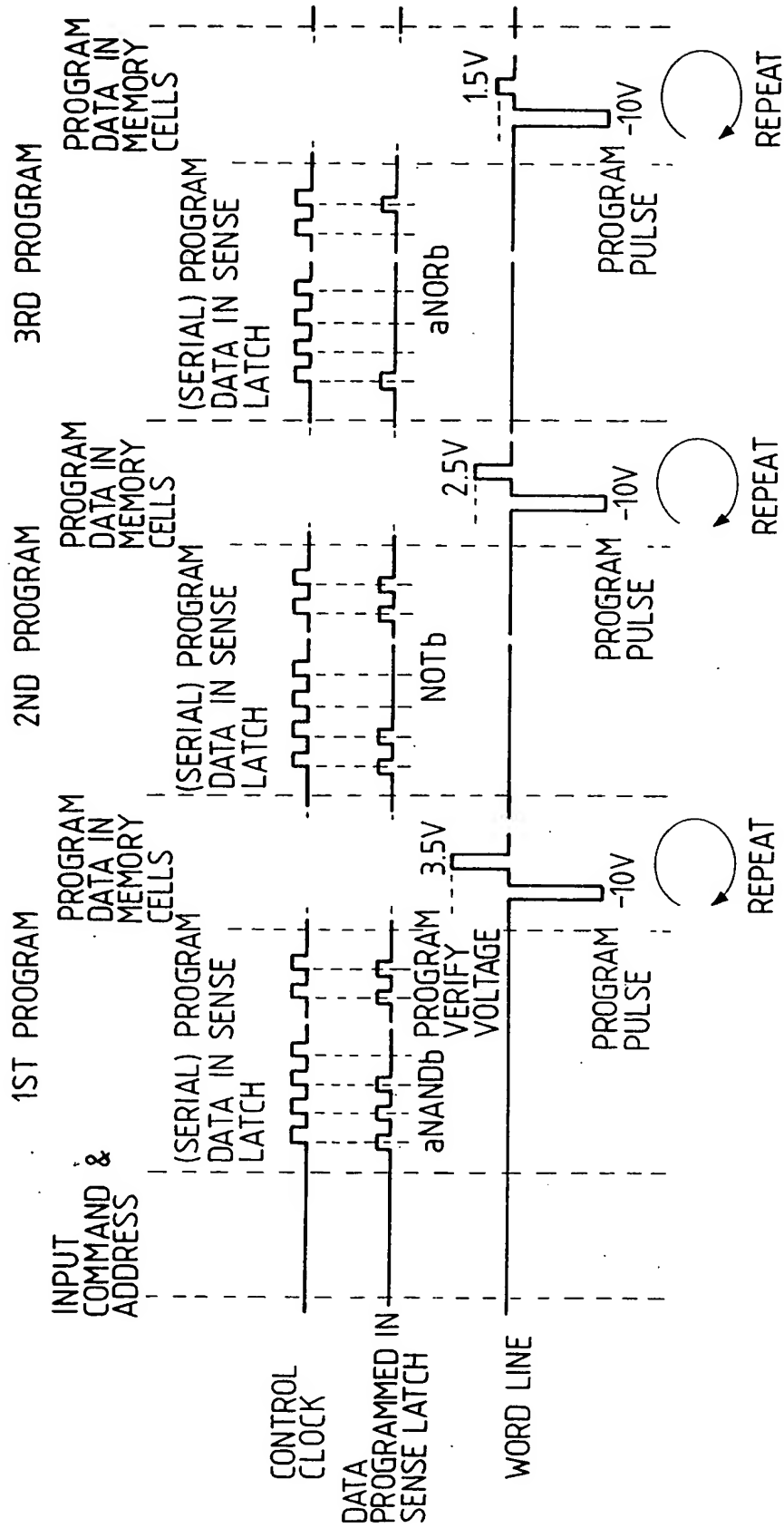


FIG. 7

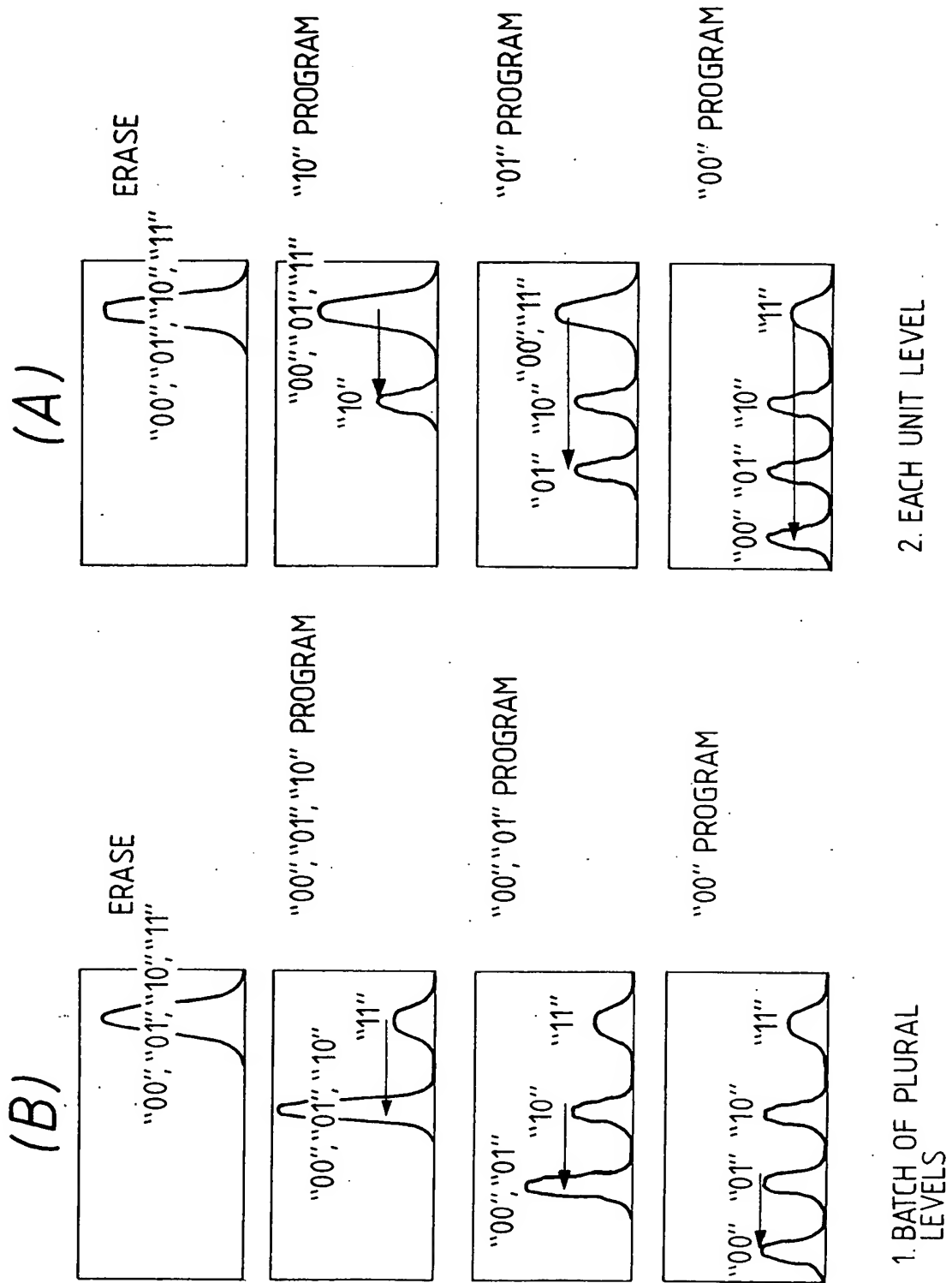


FIG. 8

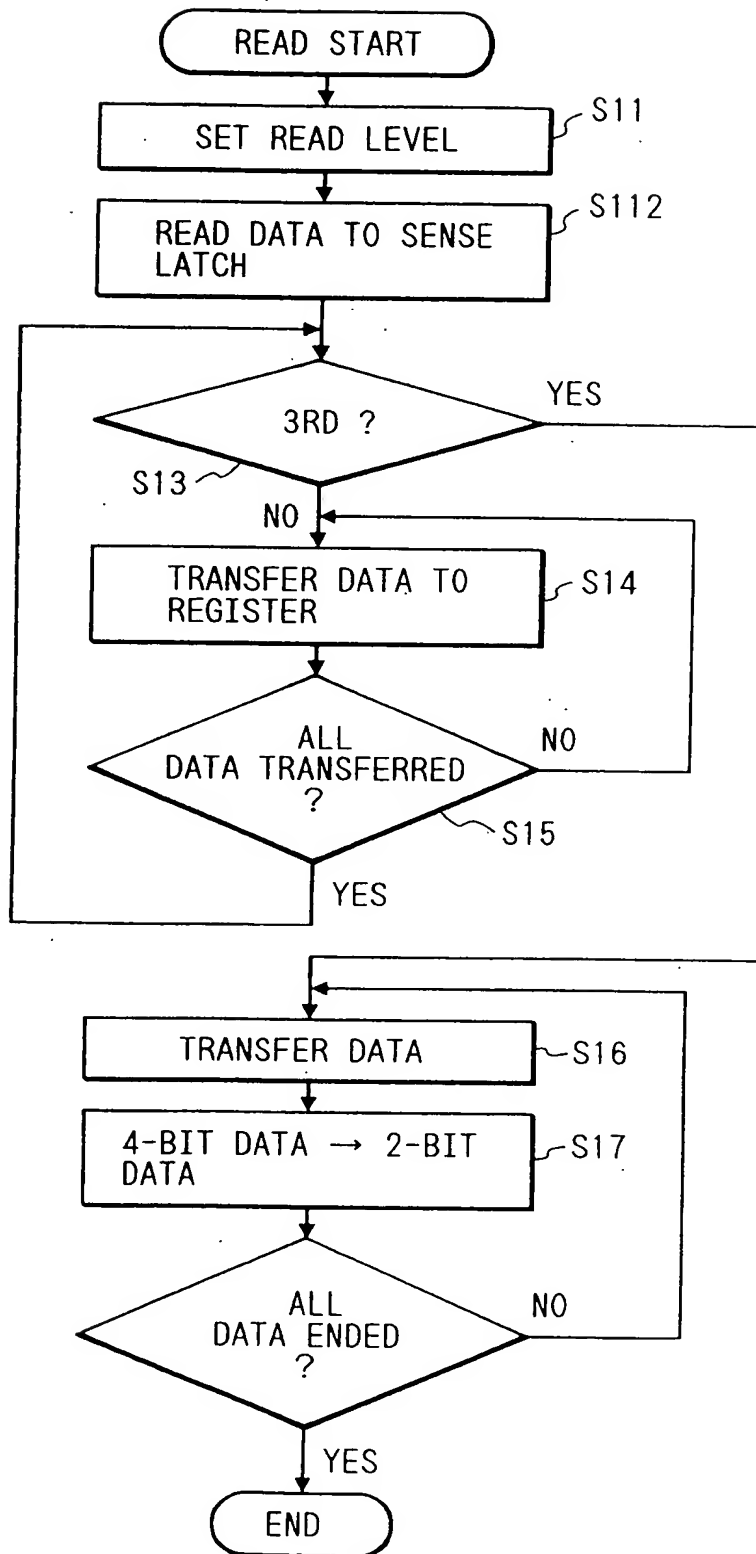


FIG. 9

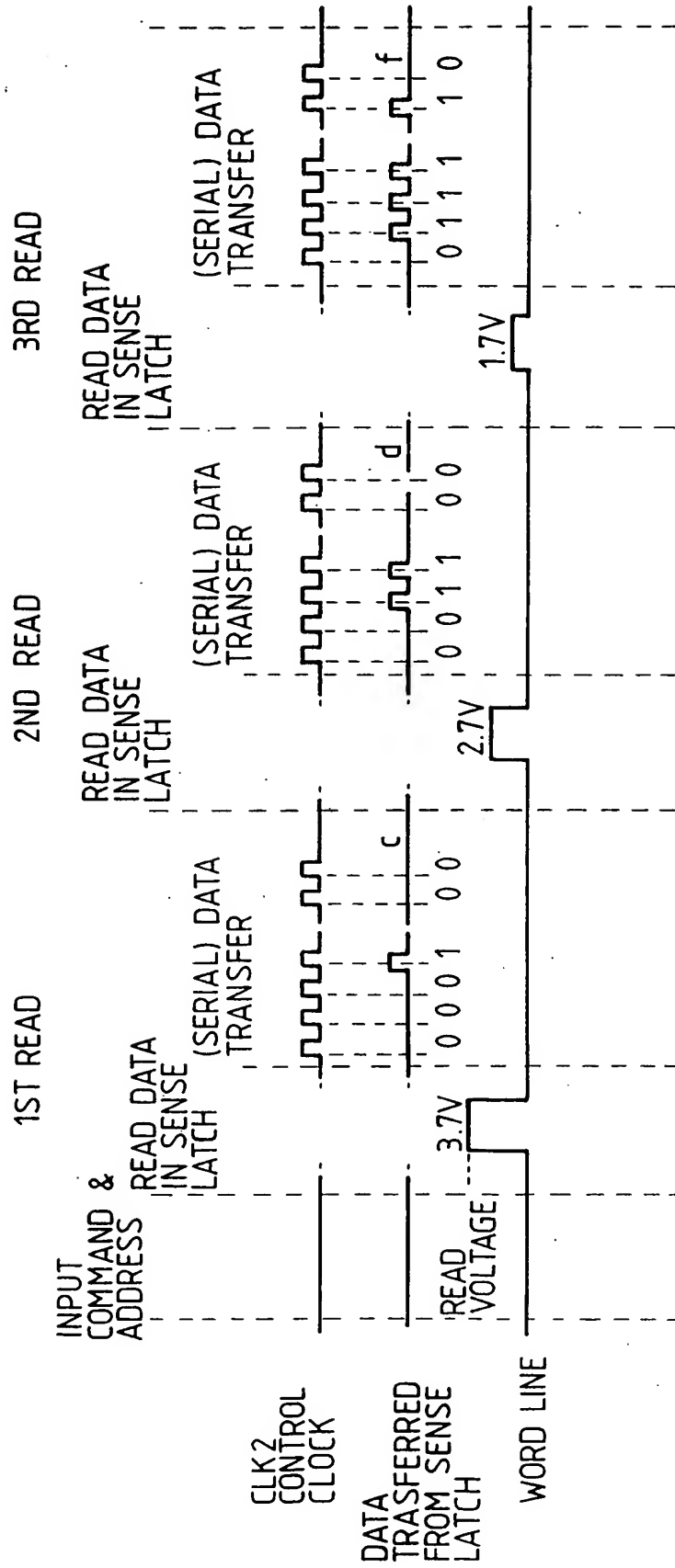




FIG. 10

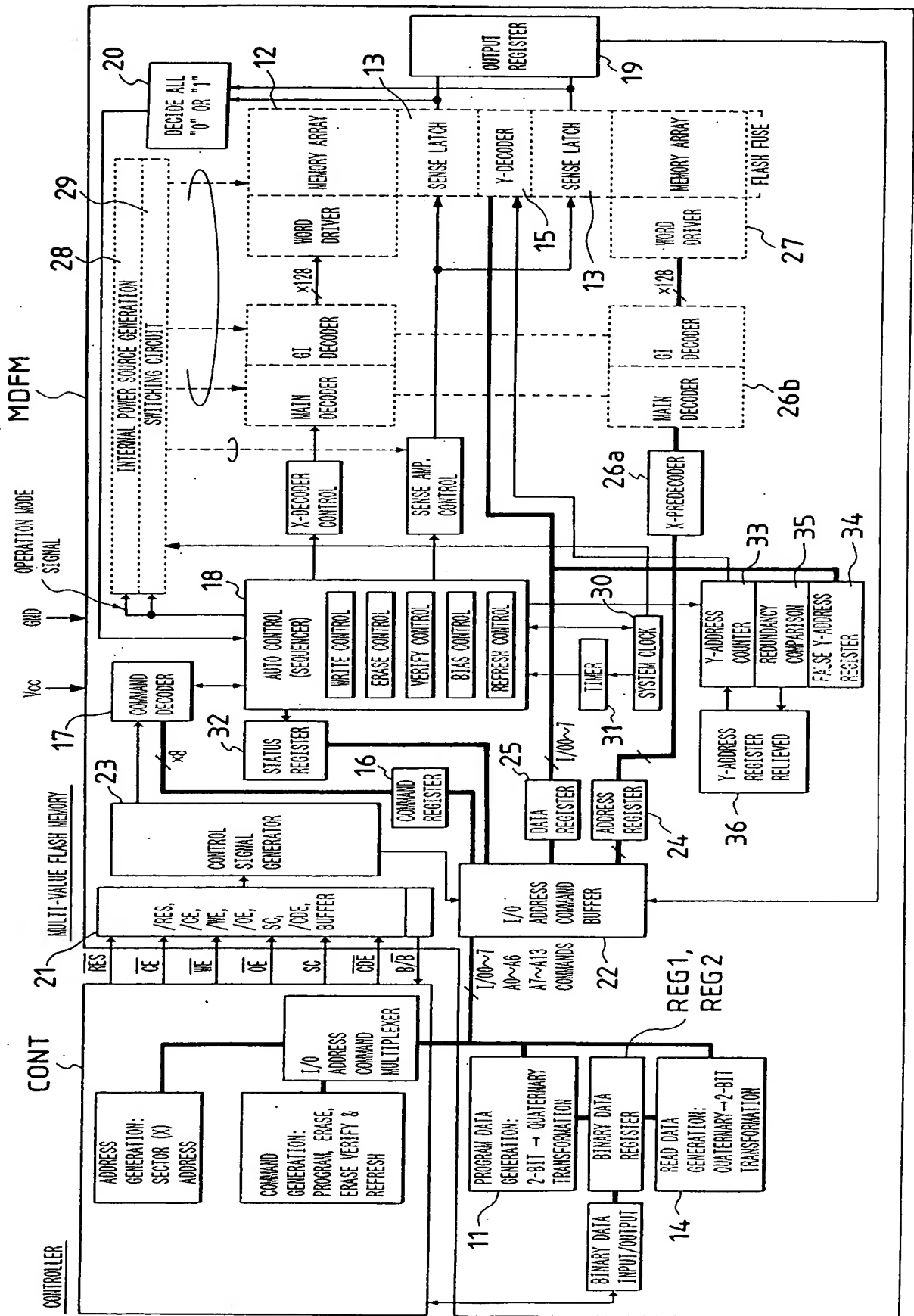
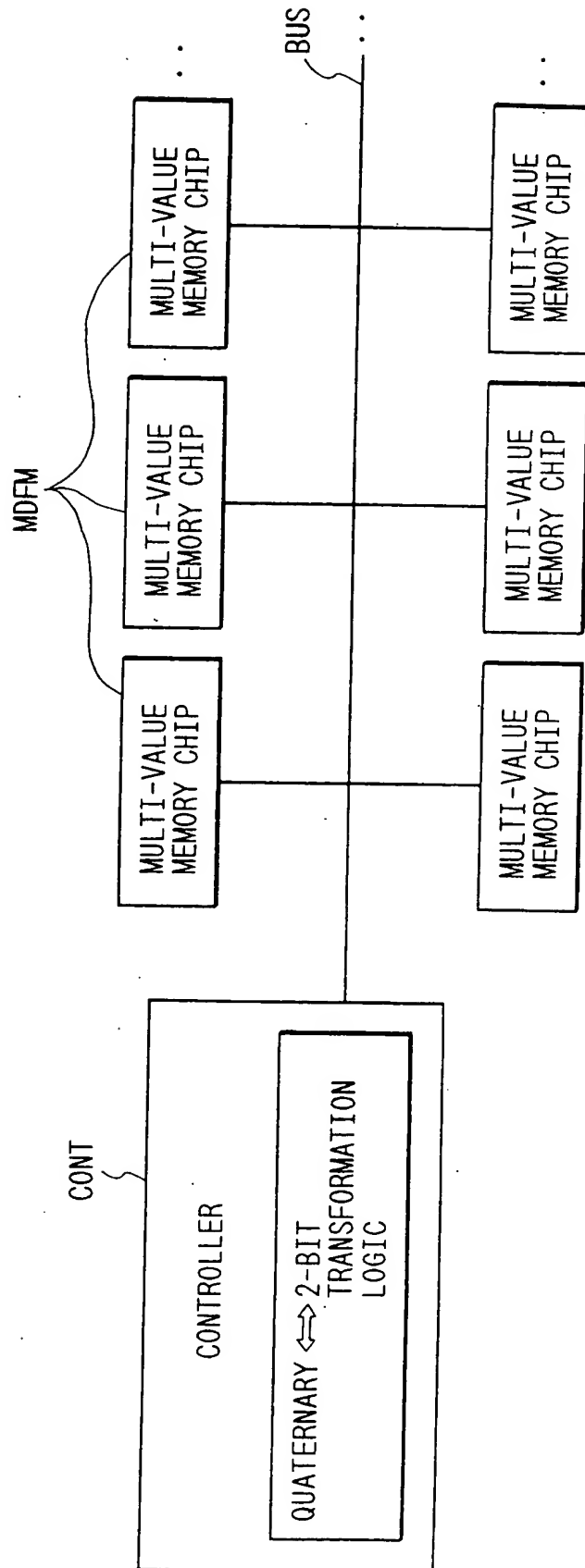


FIG. 11



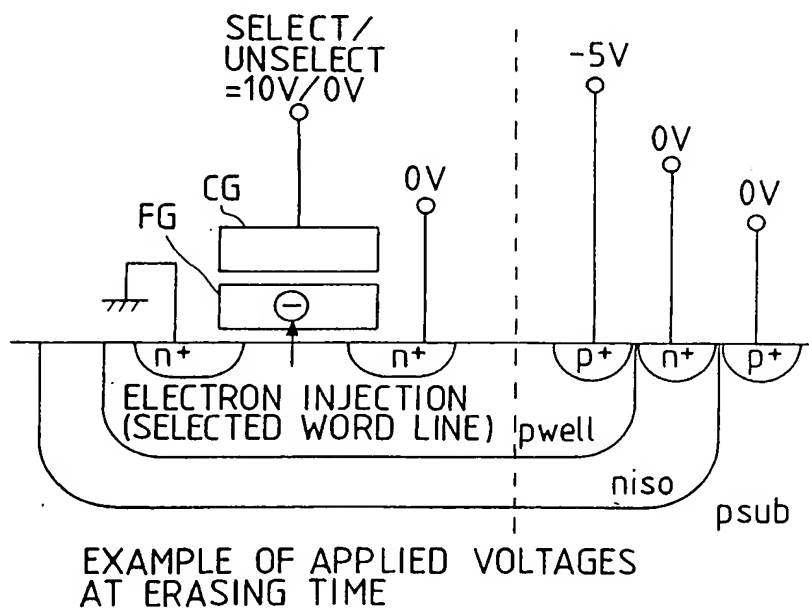


FIG. 14

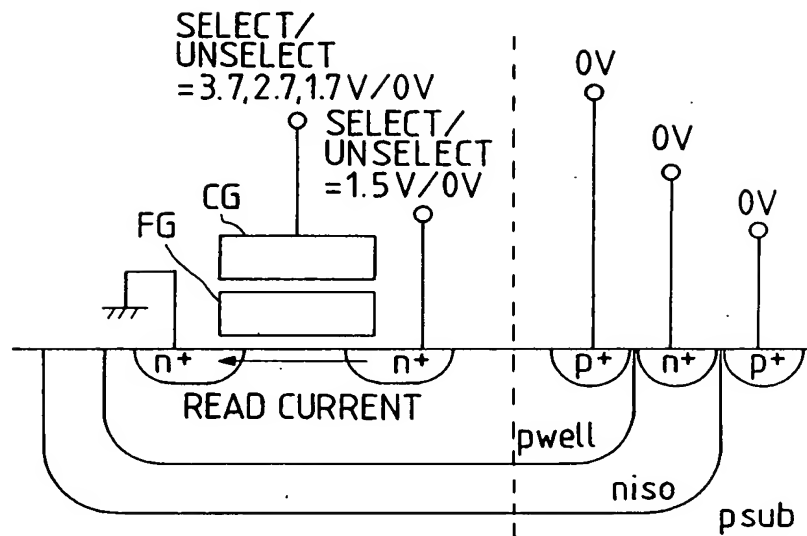
EXAMPLE OF APPLIED VOLTAGES  
AT READING TIME

FIG. 15

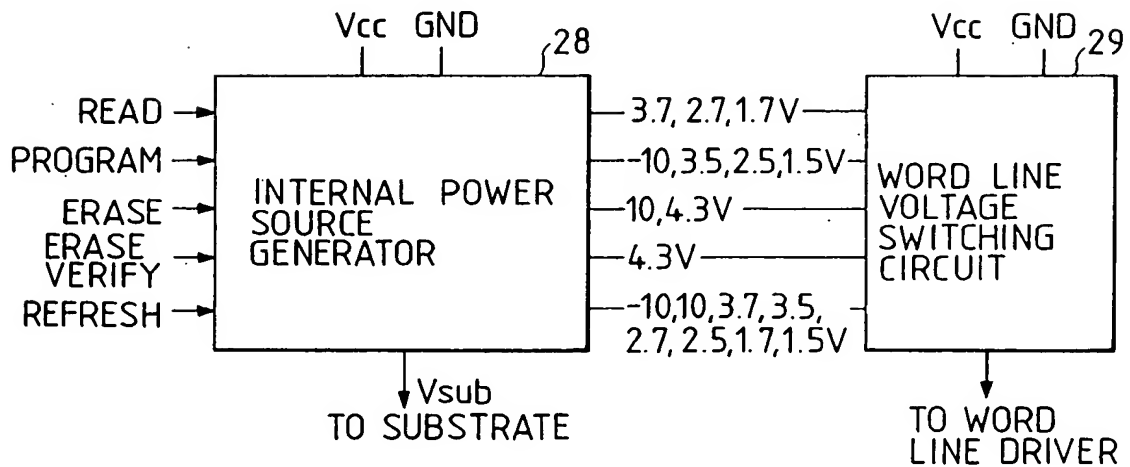


FIG. 16

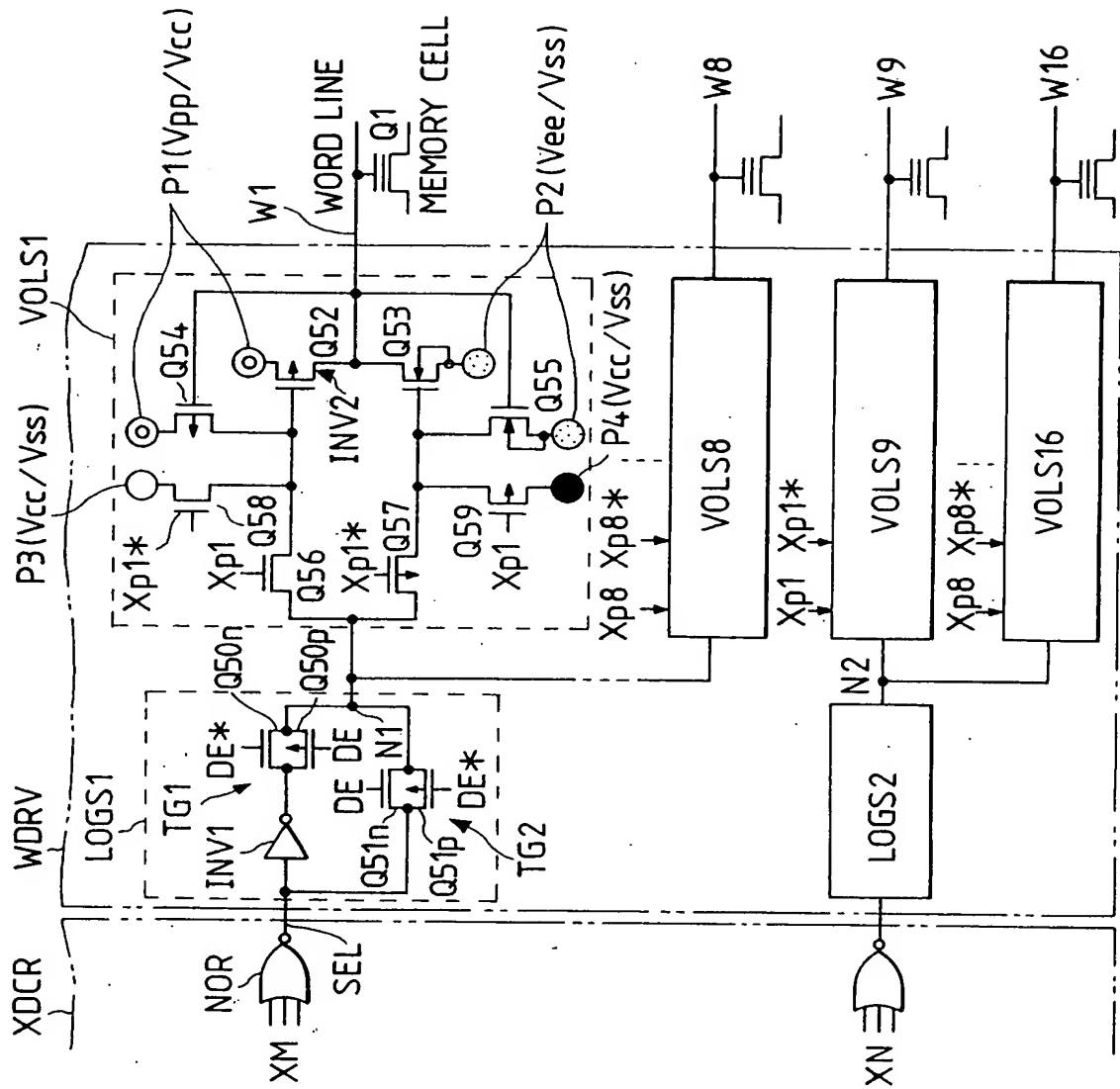


FIG. 17

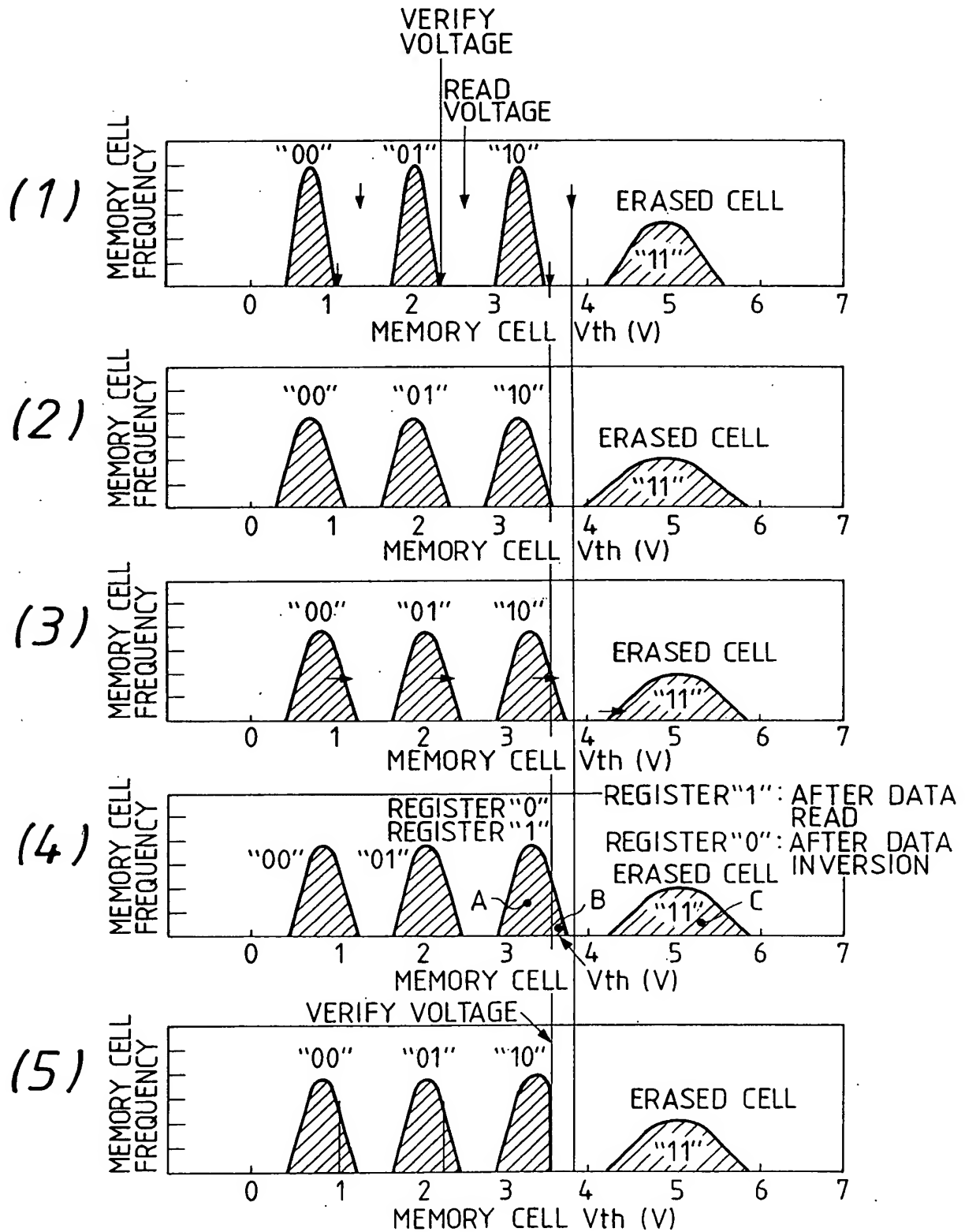


FIG. 18

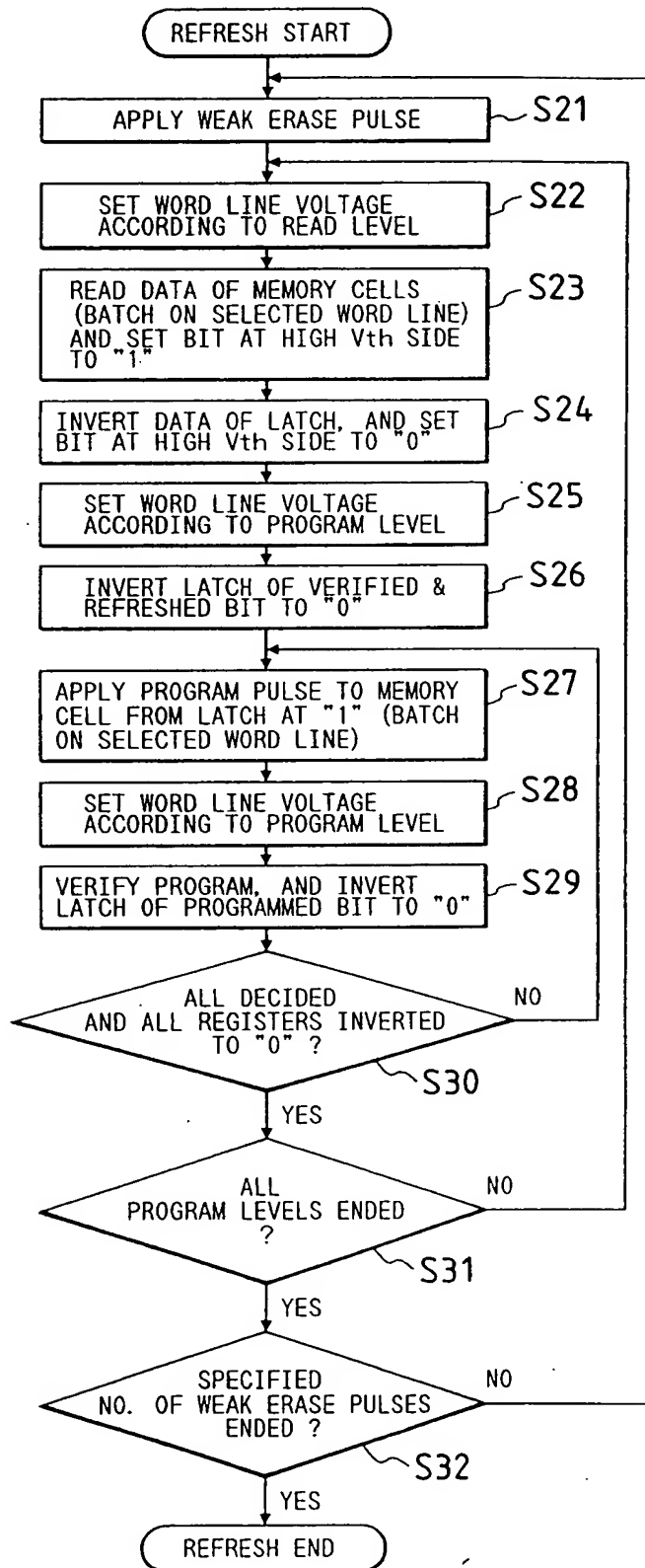


FIG. 19

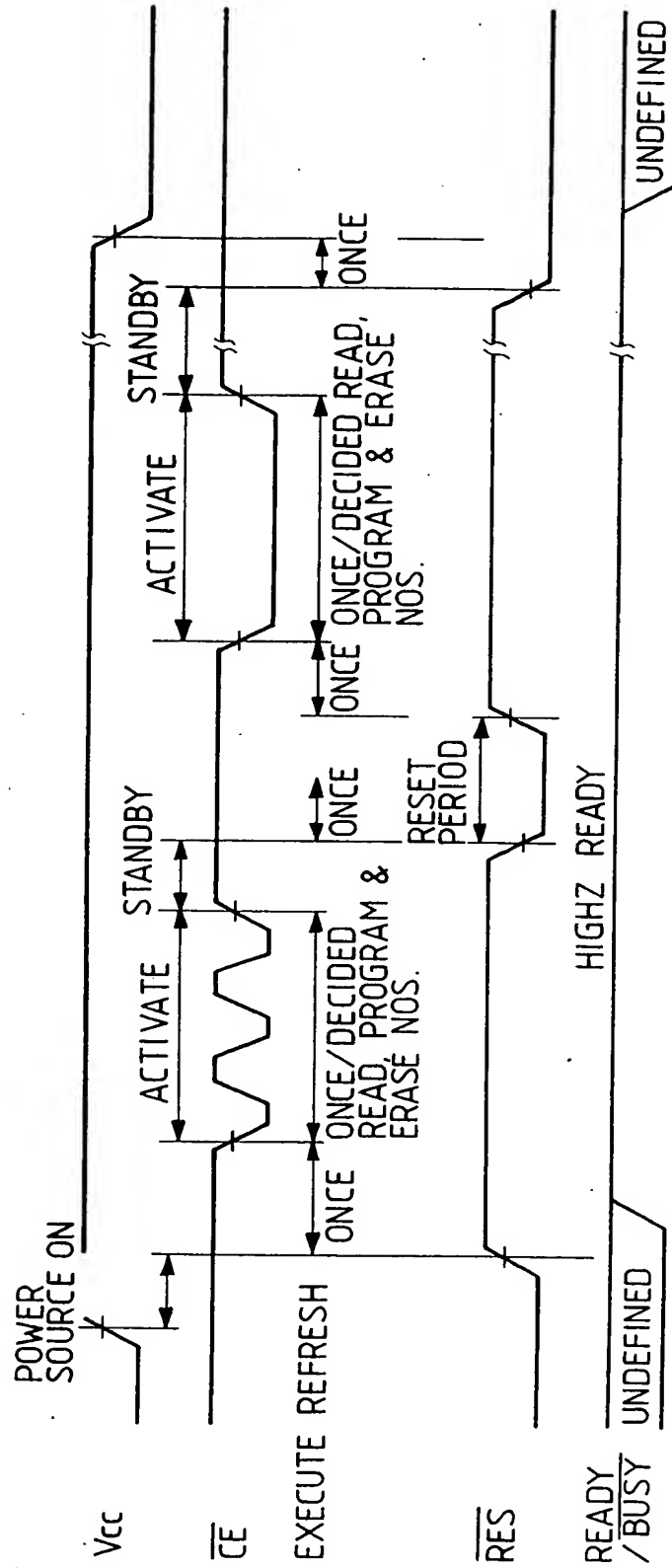




FIG. 20

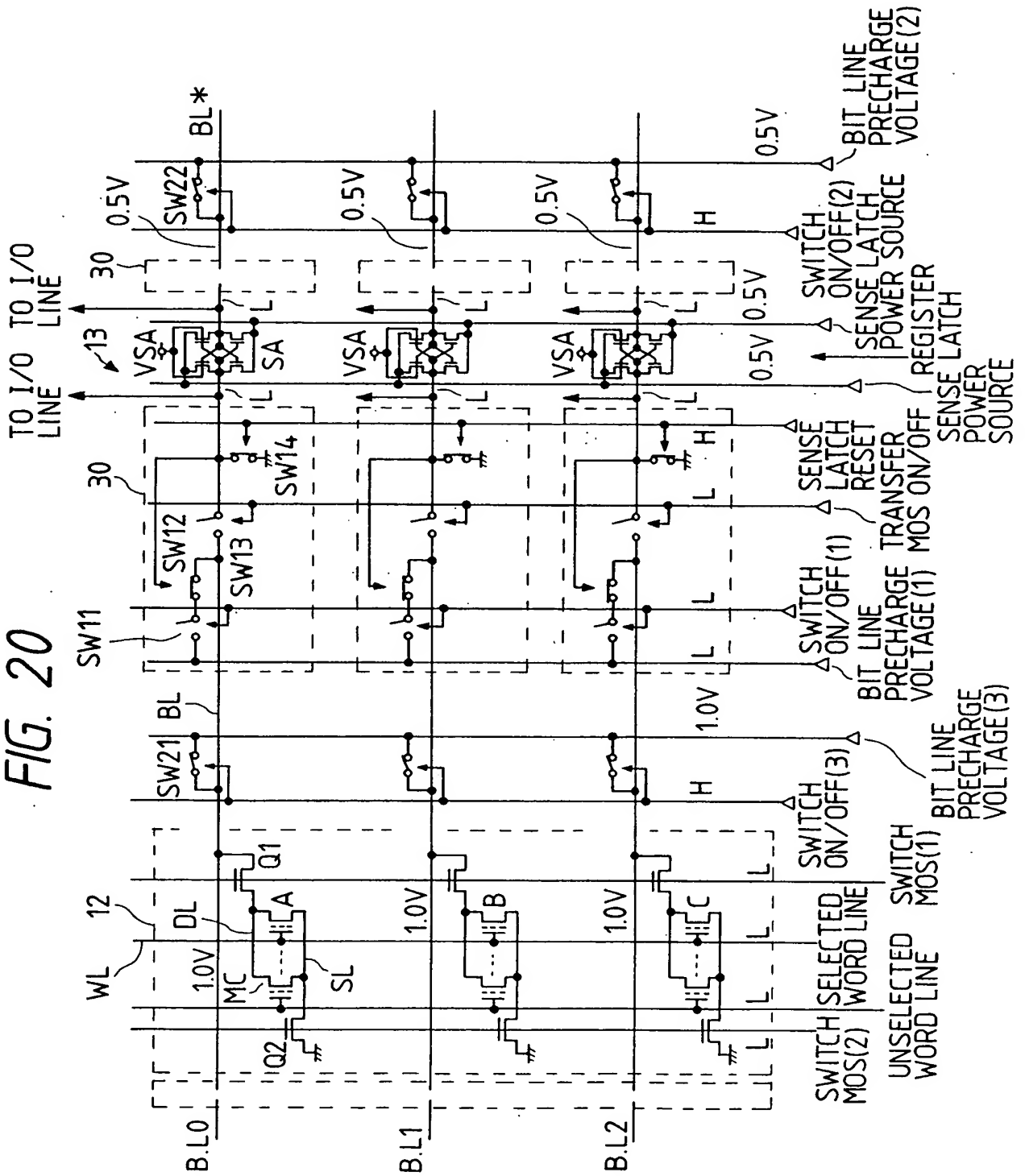


FIG. 21

